2

Transistors

CHAPTER OBJECTIVES

After studying this chapter the student will be able to:

- Explain operation of *pnp* and *npn* transistors.
- Sketch the common-base, common-emitter and common-collector characteristics.
- Compare the different transistor configurations.
- Draw the dc load line and fix bias point.
- Explain different bias circuits
- Design bias circuits for a given operating point.
- Analyze concept of thermal runway
- Realize importance of stability factor
- Compute voltage gain and current gain for common-emitter amplifier.

Transistor was invented by W.H. Brattain, John Bardeen and William Shockley in 1947. The word transistor was derived from transfer resistor, as they transfer signals from low resistance to high resistance. It is a three-layer semiconductor device in which an *n*-type semiconductor is sandwiched between two *p*-type layers or a *p*-type semiconductor is sandwiched between two *n*-type layers. It is extensively used in amplifiers, digital switches and oscillator circuits.

2.1 TRANSISTOR CONSTRUCTION

A transistor has three terminals, namely emitter (*E*), base (*B*) and collector (*C*). We have two types of transistors, *npn* and *pnp*. These are shown in Fig. 2.1.

The emitter is heavily doped and injects a large number of majority carriers into the base. The emitter is always forward biased with respect to the base. In *pnp* transistors, majority carriers are holes and in *npn* transistors, majority carriers are electrons.

electrons are collected by the collector. A few electrons also flow out of the base terminal. The BE bias voltage must be greater than the forward voltage drop of 0.7 V at the BE junction.

2.2.2 *pnp* Transistor

A *pnp* transistor behaves exactly the same way as an *npn* transistor, with the difference that the majority carriers are holes. Here too, the base is lightly doped compared to the emitter and collector. The BE junction is forward biased and CB junction reverse biased as shown in Fig. 2.5.
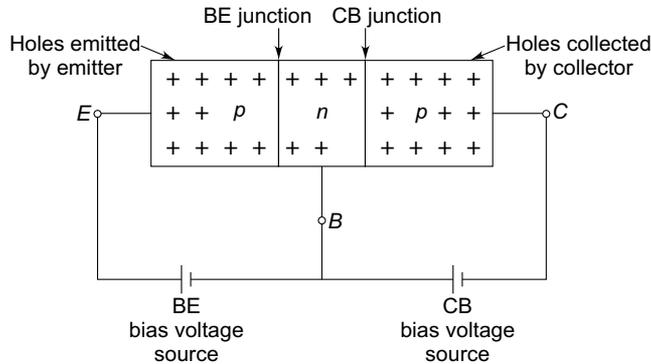

Fig. 2.5 *pnp transistor*

Holes emitted from the *p*-type emitter are injected into the base. Some of the holes flow out through the base. Most of them are collected by the collector. The BE junction bias voltage controls the large emitter and collector current.

2.3 TRANSISTOR VOLTAGES

The polarities of the terminals are important when we define the voltages of the transistor. The bias voltage sources are connected to the transistor via resistors. The base bias source is designated V_{BB} (or V_B) and connected to the base terminal through R_B. The collector bias voltage source is designated V_{CC} and is always much larger than V_{BB}, to ensure that the CB junction is reverse biased. The voltages are shown in Fig. 2.6 for an *npn* transistor.
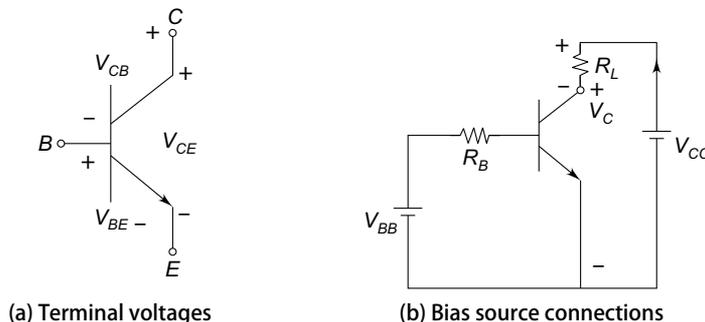

(a) Terminal voltages   (b) Bias source connections

Fig. 2.6 *Transistor voltages for npn transistor*

Note that the base is biased positive with respect to emitter. In a *pnp* transistor the base is biased negative with respect to emitter. The voltages and source connections are shown in Fig. 2.7.
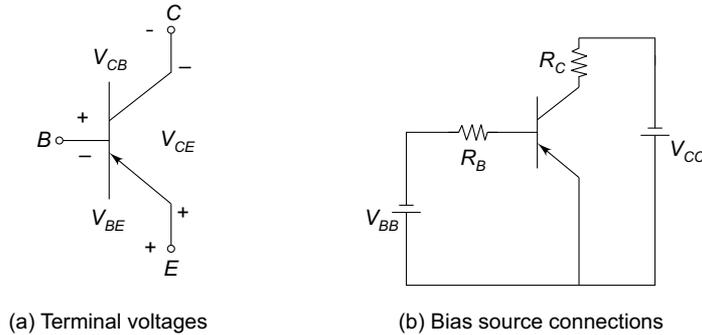

(a) Terminal voltages

(b) Bias source connections

Fig. 2.7 *Transistor voltages for pnp transistor*

2.4 TRANSISTOR CURRENTS

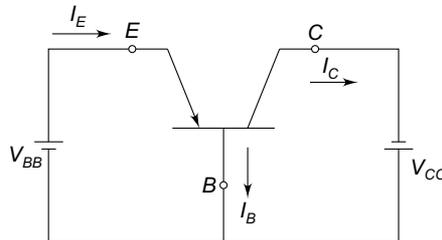Consider the *pnp* transistor with currents as shown in Fig. 2.8.

Fig. 2.8 *Currents in a pnp transistor*

The current flowing into the emitter terminal is I_E; the current flowing out of the base is I_B and out of the collector is I_C. The currents shown are the conventional currents. Here I_B and I_C flow out of the transistor and I_E flows into the transistor. Hence,

$$I_E = I_C + I_B \tag{2.1}$$

Most of the emitter current reaches the collector. Generally, the collector current is around 96% – 99.5% of emitter current. We can write,

$$I_C = \alpha_{dc} \, I_E \tag{2.2}$$

α_{dc} is the emitter-to-collector current gain and is given by

$$\alpha_{dc} = \frac{I_C}{I_E} \tag{2.3}$$

The value of α lies between 0.96 to 0.995. In circuit analysis often I_C is assumed to be equal to I_E. Due to the collector-base reverse bias, a small reverse saturation current (I_{CBO}) flows across the junction. I_{CBO} is called the collector-to-base leakage current. Substituting (2.1) in (2.2) we get

$$I_C = \alpha_{dc} (I_C + I_B) \tag{2.4}$$

$$I_C(1 - \alpha_{dc}) = \alpha_{dc} I_B$$

$$I_C = \frac{\alpha_{dc}}{1 - \alpha_{dc}} I_B \tag{2.5}$$

$$I_C = \beta_{dc} I_B \tag{2.6}$$

where $$\beta_{dc} = \frac{\alpha_{dc}}{1 - \alpha_{dc}} = \frac{I_C}{I_B} \tag{2.7}$$

β_{dc} is the base-to-collector current gain. It ranges typically from 25 to 300. From eq. (2.7) we can also obtain

$$\alpha_{dc} = \frac{\beta_{dc}}{1 + \beta_{dc}} \tag{2.8}$$

The currents in an *npn* transistor are shown in Fig. 2.7.
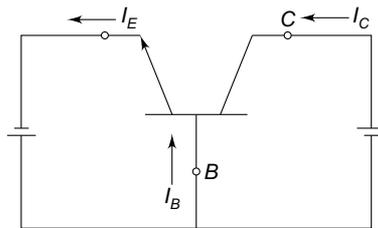

Fig. 2.9 *Currents in an npn transistor*

Here, the base and collector currents enter the transistor and the emitter current leaves the transistor. These are the directions of the conventional currents. All equations from (2.1) to (2.8) are the same.

Example 2.1 Calculate I_C, I_E and I_B for a transistor whose $\alpha_{dc} = 0.9$ and $I_B = 50$ μA. What is β_{dc}?

Solution

$$I_C = \frac{\alpha_{dc}}{1 - \alpha_{dc}} I_B$$

$$= \frac{0.9 \times 50 \times 10^{-6}}{1 - 0.9} = 0.45 \text{ mA}$$

$$I_E = \frac{I_C}{\alpha_{dc}} = \frac{0.45 \times 10^{-3}}{0.9} = 0.5 \text{ mA}$$

$$\beta_{dc} = \frac{\alpha_{dc}}{1 - \alpha_{dc}} = \frac{0.9}{1 - 0.9} = 9$$

Example 2.2   Calculate I_B, α_{dc} and β_{dc} for transistor that has $I_C = 3$ mA and $I_E = 3.5$ mA.
Solution

$$\alpha_{dc} = \frac{I_C}{I_E} = \frac{3 \text{ mA}}{3.5 \text{ mA}} = 0.857$$

$$\beta_{dc} = \frac{\alpha_{dc}}{1 - \alpha_{dc}} = \frac{0.857}{1 - 0.857} = 5.999$$

$$I_B = \frac{I_C}{\beta_{dc}} = \frac{3 \text{ mA}}{5.999} = 0.5 \text{ mA}$$

Example 2.3   For a transistor with $\alpha_{dc} = 0.99$, $I_B = 100$ μA, determine I_C
Solution

$$\beta_{dc} = \frac{\alpha_{dc}}{1 - \alpha_{dc}} = \frac{0.99}{1 - 0.99} = 99$$

$$I_C = \beta_{dc} I_B = 99 \times 100 \times 10^{-6} = 9.9 \text{ mA}.$$

Example 2.4   Consider a transistor that has a collector current of 3 mA and emitter current of 3.03 mA. Calculate the new currents if the transistor is replaced by a new device that has $\beta = 75$, if the base current is unchanged.
Solution

$$\alpha_{dc} = \frac{I_C}{I_E} = \frac{3 \times 10^{-3}}{3.03 \times 10^{-3}} = 0.99$$

$$\beta_{dc} = \frac{\alpha_{dc}}{1 - \alpha_{dc}} = \frac{0.99}{1 - 0.99} = 99$$

$$I_B = \frac{I_C}{\beta_{dc}} = \frac{3 \times 10^{-3}}{99} = 30 \ \mu A$$

If $\beta_{dc} = 75$,

$$I_C = \beta_{dc} I_B = 75 \times 30 \ \mu A = 2.25 \ mA$$

$$\alpha_{dc} = \frac{\beta_{dc}}{1 + \beta_{dc}} = \frac{75}{1 + 75} = 0.98$$

$$I_E = \frac{I_C}{\alpha_{dc}} = \frac{2.25 \times 10^{-3}}{0.98} = 2.29 \ mA$$

2.5 CURRENT AND VOLTAGE AMPLIFICATION

A small change in the base current produces a large change in the emitter and collector currents. We can define the base to collector gain as

$$\beta_{dc} = \frac{\Delta I_C}{\Delta I_B}$$

Lower case letters are used to represent ac quantities.

$$\beta_{ac} = \frac{I_c}{I_b} \tag{2.9}$$

In data sheets β_{dc} is normally represented as h_{FE} and β_{ac} by h_{fe}

Considering Fig. 2.6b, $V_C = V_{CC} - I_C R_L$. If the base current changes by a value ΔI_B, the collector changes by $\Delta I_C = \beta_{dc} \Delta I_B$. The change in collector current causes a variation in the transistor collector voltage, $\Delta V_C = \Delta I_C R_L$. The voltage gain is given by

$$A_V = \frac{\Delta V_C}{\Delta V_B} \tag{2.10}$$

2.6 COMMON BASE CHARACTERISTICS

The performance of the transistor in a circuit, depends on the *V–I* characteristics of the transistor. The transistor is a three-treminal device. One terminal is made common to input and output. The other two will be the other input terminal and the output terminal. Based on which terminal is made common, we have

- Common base
- Common emitter
- Common collector configurations

In common base configuration, the base terminal is common to input and output voltages as shown in Fig. 2.10, for a *pnp* transistor. Ammeters and voltmeters are added to indicate the measurement set up.
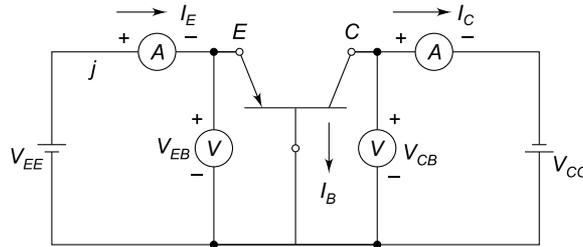

Fig. 2.10   *Common base configuration*

Here note the following:

$$I_E = I_C + I_B$$

V_{EB} is positive (input voltage)
V_{CB} is negative (output voltage)

2.6.1   Input Characteristics

The input characteristics give the relationship between the input voltage, V_{EB} and the input current, I_E for a constant output voltage. Since the input p-n junction is a forward biased diode, the input characteristics are similar to the forward bias characteristics of a diode as shown in Fig. 2.11.
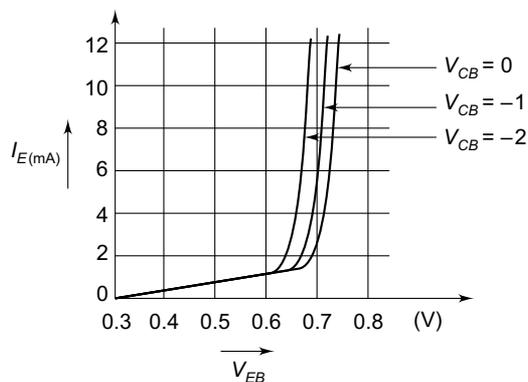

Fig. 2.11   *Input characteristics of CB configuration*

The following points may be noted from the characteristics:

1. The emitter current I_E, increases as the input forward bias voltage, V_{EB}, is increased. Before the cut-in voltage the current is minimum and increases as the input voltage increases.

2. When the reverse bias on CB junction increases, the current increases for a given level of input voltage. This is because as the reverse bias voltage is increased, the depletion region penetrates deeper into the base facilitating more carrier collection due to reduction in resistance between the EB and CB depletion regions.
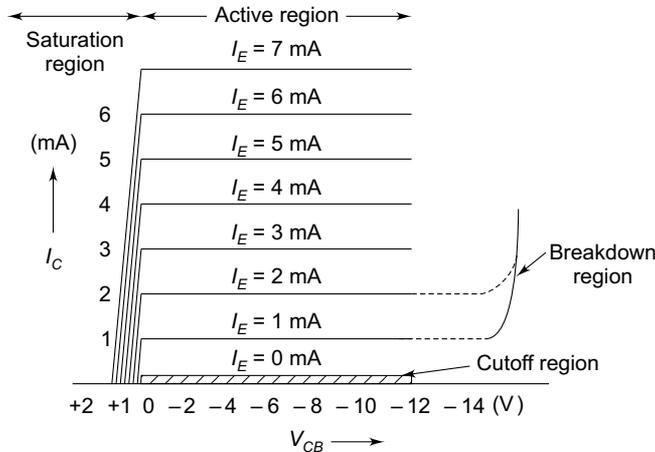
2.6.2 Output Characteristics

Fig. 2.12 *Output characteristics of CB configuration*

To determine the output characteristics, emitter current I_E, is kept constant by applying a fixed input voltage V_{EB}. Then the reverse bias of V_{CB} is increased and the collector current observed for each value of V_{CB}. This is repeated for different values of input current and plotted as shown in Fig. 2.12. The output current I_C remains almost constant and is approximately equal to I_E, even with increase in V_{CB}.

The set of curves has different regions of operation as indicated in Fig. 2.12. They are described next.

Active region: In this region EB junction is forward biased and CB junction is reverse biased. When emitter current $I_E = 0$, the collector current will be equal to the reverse saturation current I_{CBO} of the CB junction. When emitter current I_E flows, a fraction $\alpha_{dc} I_E$ flows through the collector. Since α is $\cong 1$, $I_C = I_E$. In this region the collector current depends only on I_E and is almost independent of V_{CB}. However, for a large change in V_{CB} there is a small increase in collector current because of decrease in the base width. This reduction in the base width also reduces I_B.

Saturation region: Even when V_{CB} is reduced to zero, the current I_C still flows. This is because the barrier voltage across the CB junction assists the flow of minority carriers across the CB junction. To reduce the collector current to zero, the CB junction has to be forward biased. When V_{CB} is positive the CB junction is forward biased and for a slight increase of V_{CB} in positive direction current decreases to zero. This region where both EB and CB junctions are forward biased is called the *saturation region*

Breakdown region: If the reverse bias of CB junction is increased beyond the limit specified for the device, breakdown occurs. This can also occur if the depletion region of the CB reverse bias junction penetrates into base until it makes contact with depletion region of EB junction. This is called punch-through wherein very large currents can flow damaging the device.

Cut-off region: When the EB and CB junctions both are reverse biased, the transistor operates in the cut-off region. Here $I_C = 0$.

2.6.3   Current Gain Characteristics

They are also termed forward transfer characteristics and are a plot of I_C V_s I_E for different values of V_{CB}. The plot is shown in Fig. 2.13. An increase in reverse bias of V_{CB} only increases the collector current very slightly. The slope is Ω 1.
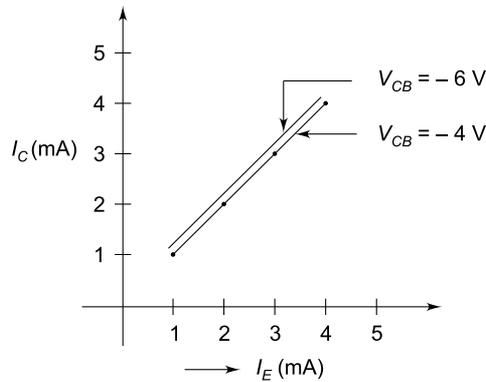

Fig. 2.13   *Transfer characteristics of CB configuration*

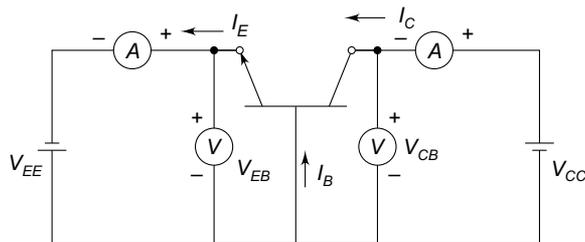The common base configuration for an *npn* transistor is shown in Fig. 2.14.

Fig. 2.14   *Common base configuration for npn transistor*

Here, the source V_{EE} and V_{CC} are connected as shown. V_{EB} is negative (with polarities as shown) and V_{CB} is positive. The characteristics are identical to Fig. 2.11, 2.12 and 2.13.

2.7   COMMON EMITTER CHARACTERISTICS

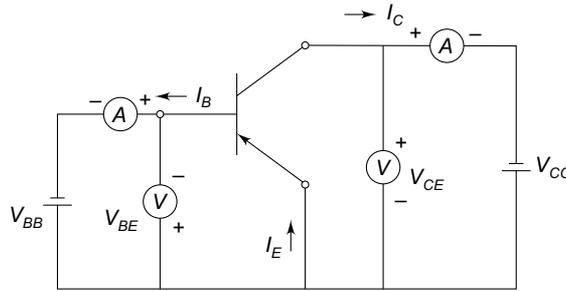The common emitter configuration is shown in Fig. 2.15 for a *pnp* transistor.

Fig. 2.15 *Common emitter configuration for a pnp transistor*

Note the following with respect to Fig. 2.15.

- $I_E = I_C + I_B$
- Emitter terminal is common to input and output.
- V_{BE} is input voltage (with polarities shown). It is positive.
- V_{CE} is output voltage. It is negative for the polarities shown.

2.7.1 Input Characteristics

The input characteristics is a plot of V_{BE} V_S I_B at constant V_{CE}. The characteristics is similar to that of a forward biased diode. I_B is only a small portion of the total emitter current that flows across forward biased base-emitter junction. The characteristics are as shown in Fig. 2.16.
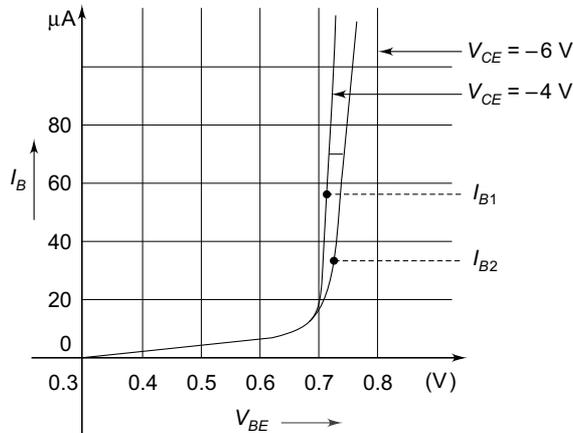

Fig. 2.16 *Input characteristics of CE configuration*

We can observe from Fig. 2.14 that for the same value of V_{BE} the base current (I_{B1}) is more with lesser reverse bias voltage, V_{CE} (−4V) as compared to higher reverse bias voltage (−6V). This is because as reverse bias is increased, the depletion layer of CB junction penetrates deeper into the base, facilitating better collection of majority charge carriers, thus increasing I_C. Since $I_B = I_E − I_C$, I_B is reduced. Reduction in base width due to changes in V_{CE} is called *early effect*.

2.7.2   Output Characteristics

The output characteristics is a plot of I_C V_S V_{CE}, for constant values of I_B, as shown in Fig. 2.17. Here I_B (and not I_E) is held constant. Hence, as V_{CE} is increased, the shortening of the depletion regions of base-emitter junction and collector-base junction, increases the collector current. The various regions are as follows:
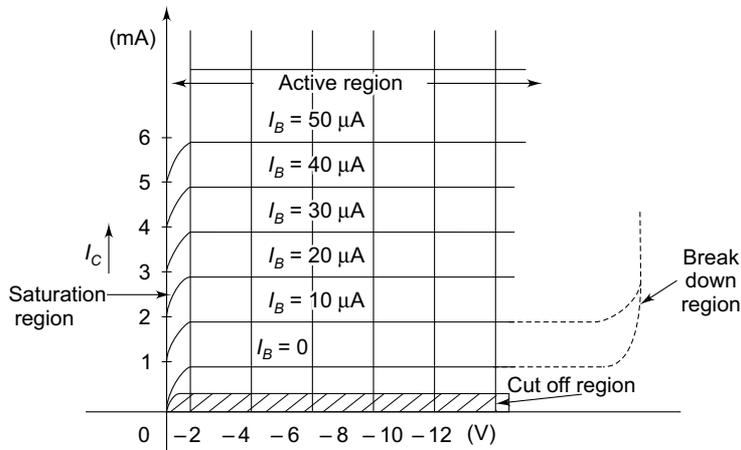

Fig. 2.17   *Output characteristics of CE configuration for a pnp transistor*

The different regions of operation are as follows:

Active region

In this region the emitter-base junction is forward biased and the collector-base junction is reverse biased. The voltage V_{CE} should reach a level where V_{CB} (collector-base voltage) is sufficient to reverse bias CB junction.

Cut-off region

In common base configuration when $I_E = 0$, I_C is equal to the reverse saturation current I_{CBO}, which is practically zero. However, in common emitter configuration, I_C is not equal to zero even though $I_B = 0$. We know,

$$I_C = \alpha I_E + I_{CBO}$$

$$I_C = \alpha(I_C + I_B) + I_{CBO}$$

$$I_C = \frac{\alpha I_B}{1 - \alpha} + \frac{I_{CBO}}{1 - \alpha} \tag{2.11}$$

If $I_B = 0$, $I_C = \dfrac{I_{CBO}}{1 - \alpha}$. Since α is close to 1(around 0.995), I_C will be significant even if $I_B = 0$. We denote as

$$I_{CEO} = \left.\frac{I_{CBO}}{1 - \alpha}\right|_{I_B = 0\mu A}$$

In common-emitter we can define cut-off as the point where $I_C = I_{CEO}$. So we need to avoid operation below $I_B = 0\mu A$. Equation (2.11) can be written as

$$I_C = \beta I_B + (\beta + 1)\, I_{CBO} \tag{2.12}$$

Saturation region

In this region both junctions are forward biased. The majority carriers emitted from emitter will face repulsion from the collector which is forward biased (for low values of V_{CE}) and I_C reduces to zero.

Breakdown region

In this region the reverse bias of CB junction is increased to such an extent that the junction breaks down.

2.7.3 Current Gain Characteristics

The current gain characteristics for common-emitter configuration is a plot of I_C V_S I_B for constant V_{CE}. It is shown in Fig. 2.18.
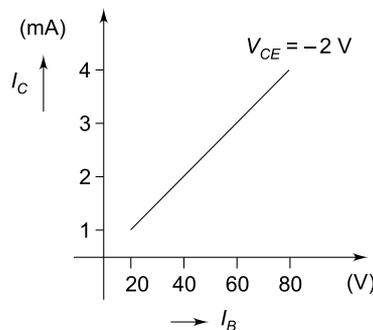

Fig. 2.18 *Current gain characteristics of CE configuration.*

2.8 COMMON COLLECTOR CHARACTERISTICS

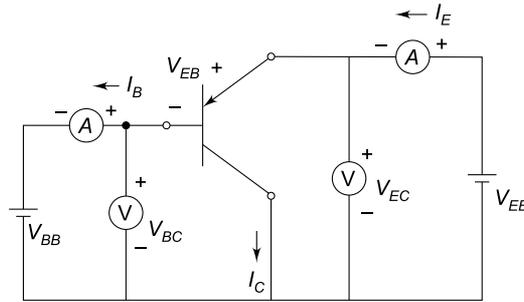In common collector configuration, the collector terminal is common to input and output as shown in Fig. 2.19.

Fig. 2.19 *Common collector configuration for pnp transistor*

Here $\qquad V_{EC} = V_{BC} + V_{EB}$

So $\qquad V_{BC} = V_{EC} - V_{EB}$

V_{BC} should be such as to make V_{EB} positive to forward bias the base-emitter junction. As V_{BC} is increased, V_{EB} decreases for constant V_{EC} and I_B decreases.

Input characteristics

As discussed, when V_{BC} is increased I_B decreases. The input characteristics shown in Fig. 2.20 is distinctly different from the input characteristics of common base and common emitter configurations.
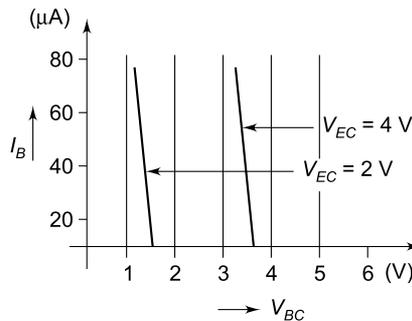

Fig. 2.20 *Input characteristics of common collector configuration*

Output characteristics

The output characteristics is a plot of I_E V$_S$ V_{EC} for constant value of I_B. Since $I_E \cong I_C$, the output characteristics and current gain characteristics are similar to the common emitter configuration as shown in Fig. 2.21.
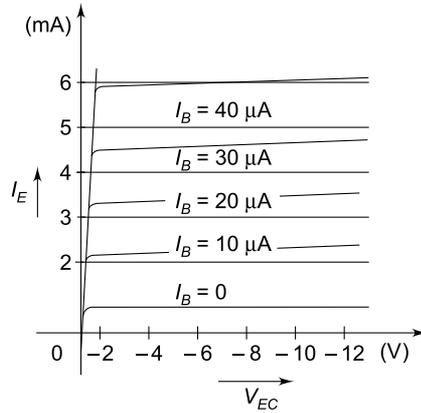
Fig. 2.21 *Output characteristics of common collector configuration*

The common collector configuration has a high input impedance and low output impedance unlike the CB and CC configurations. Hence, it is used for impedance-matching.

The common collector current gain gamma is given by

$$\gamma = \frac{\Delta I_E}{\Delta I_B} \text{ or } \frac{I_E}{I_B}$$

$$I_E = I_C + I_B = (\alpha I_E + I_{CBO}) + I_B$$

$$I_E(1 - \alpha) = I_B + I_{CBO}$$

$$I_E = \frac{I_B}{1 - \alpha} + \frac{I_{CBO}}{1 - \alpha}$$

$$= (\beta + 1) I_B + (\beta + 1) I_{CBO}$$

$$= \gamma I_B + \gamma I_{CBO} \tag{2.13}$$

$$\gamma = \beta + 1$$

Thus the current gains are all related to each other as follows:

$$\alpha = \frac{\beta}{\beta + 1}$$

$$\beta = \frac{\alpha}{1 - \alpha}$$

$$\gamma = \beta + 1.$$

The comparison of the three configurations is shown in Table 2.1.

Table 2.1 Transistor configurations

Type	CB	CE	CC
Voltage gain	High	Medium	Low
Current gain	Low (α)	High (β)	High (γ)
Power gain	Low	High	Medium
Input resistance	Low	Medium	High
Output resistance	High	Medium	Low
Applications	For high frequencies applications	Andio frequency applications	Impedance matching
Phase relationship between input and output	In-phase	Out of phase	In-phase
Output current	$I_C = \alpha I_E + I_{CBO}$	$I_C = \beta I_B + (1 + \beta) I_{CBO}$	$I_E = \gamma I_B + \gamma I_{CBO}$

2.9   LIMIT OF OPERATION

The transistor must be operated in a region where the maximum ratings are not exceeded. Some of the limits are:

1. Maximum collector current
2. Maximum collector to emitter voltage.
3. Minimum V_{CE} so the device does not go off into saturation. This is denoted by $V_{CE\,\text{sat}}$.
4. Maximum power dissipation level

$$P_{C\max} = V_{CE}\, I_C$$

5. I_C should be $> I_{CEO}$ to prevent operation in the cut-off region.

These can be summarized as

$$I_{CEO} \leq I_C \leq I_{C\max}$$

$$V_{CE\,\text{sat}} \leq V_{CE} \leq V_{CE\max}$$

$$V_{CE}\, I_C \leq P_{C\max}$$

2.10   TRANSISTOR BIASING

The analysis of transistor circuits requires a knowledge of both the ac and dc response of the system. Though the dc response can be separated, the choice of parameters for one affects the performance of the other. Biasing is the process of providing dc voltages to operate the transistor in the desired region required for the particular application. In any biasing network we use the following approximate relationships:

$$V_{BE} = 0.7 \text{ V}$$

$$I_E \cong I_C$$

$$I_E = (\beta + 1) I_B$$

$$I_C = \beta I_B$$

$$I_C = \alpha I_E$$

The biasing network fixes the operating point or quiescent point (Q – point).

We need to keep in mind that to bias a *p-n* junction the following polarities have to be maintained:

- To forward bias *p* is positive
- To reverse bias *p* is negative.

We can operate the transistor in the following regions

1. Active region (or linear region): Base-emitter junction is forward biased. Base-collector junction is reverse biased.
2. Cut off region: Base-emitter junction and base-collector junction are reverse biased.
3. Saturation region: Base-emitter junction and base-collector junction are forward biased.

The biasing circuit sets the operating point of the transistor. In amplifier circuits the transistor must be biased with constant dc levels of collector, base and emitter currents and terminal voltages. Amplifier circuits are common emitter circuits. The dc operating point or the quiescent point is given by dc levels of I_C and V_{CE}.

These values are affected by temperature changes and the current gain (β or h_{FE}). A stable biasing circuit should hold these values reasonably constant regardless of h_{FE} and temperature changes. To understand the biasing circuit it is essential to know about the dc load line.

2.10.1 DC Load Line
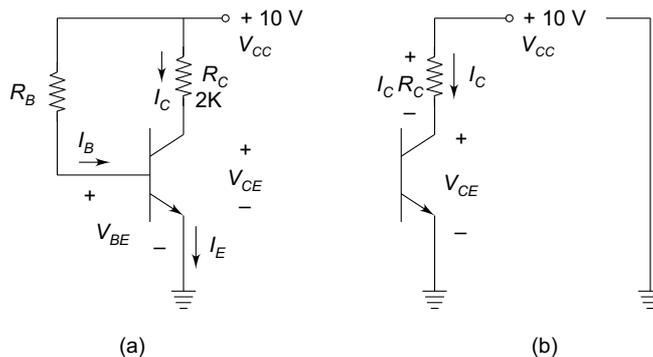
Consider the circuit of Fig. 2.22(a).

Fig. 2.22 *Transistor circuit with R_C and R_B*

The dc load line is a plot of I_C V$_s$ V_{CE} for a given value of R_C and V_{CC}. Like in the diode load line, it shows all the possible values of I_C and V_{CE} that can exist in the circuit.

From Fig. 2.22(b) we can have the equation for the output aside as

$$V_{CC} = I_C R_C + V_{CE}$$

or
$$V_{CE} = V_{CC} - I_C R_C \qquad (2.14)$$

In eq. (2.14) we consider two points.

(i) $I_C = 0$; then $V_{CE} = V_{CC}$

For the values of Fig. 2.22(a),

$V_{CE} = 10$ V

(ii) $V_{CE} = 0$; $I_C = \dfrac{V_{CC}}{R_C}$

For values chosen

$I_C = \dfrac{10V}{2K} = 5$ mA.

We now have two points of (V_{CE}, I_C), namely (10 V, 0 mA) and (0 V, 5 mA). These two points are joined by a straight line, on the output characteristics. The straight line drawn is the load line. It represents all possible values of I_C and the corresponding values of V_{CE} that can exist in the circuit. The dc load line is drawn on the output characteristics as shown in Fig. 2.23. Note however that the dc load line itself does not depend on the device characteristics and is only dependent on values of I_C and V_{CE}.
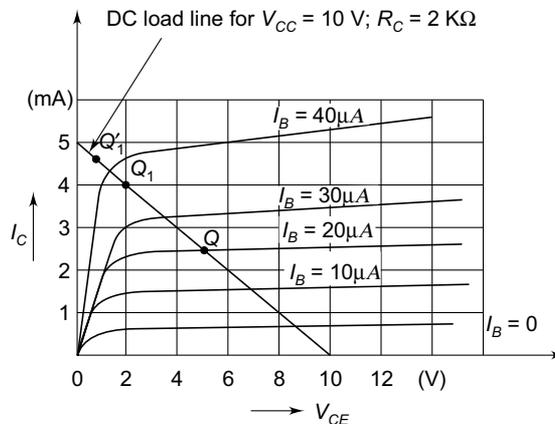

Fig. 2.23 *DC load line*

If now $I_B = 20$ μA, the Q point is as shown in Fig. 2.23. This is the dc point and no input signal is given to the base. If now an input signal is connected to the base terminal, I_B varies according to instantaneous values of the input signal. This causes I_C to vary and hence V_{CE} according to Eq. (2.14). The biasing should be such that when input swings, the operating point

$$I_C = \beta I_B = h_{FE} \, I_B = 100 \times 20 \ \mu A$$

$$= 2 \ mA$$

$$V_{CE} = V_{CC} - I_C \, R_C$$

$$= 20 - 2 \times 10^{-3} \times 2.2 \times 10^3$$

$$= 15.6 \ V.$$

The Q point varies widely with variations in h_{FE}. For a transistor of a particular type, h_{FE} varies between $h_{FE, \min}$ and $h_{FE, \max}$. This gives wide variation in I_C and V_{CE}. This has to be considered while designing the circuit.

Though simple, base bias circuit is not widely used because of its unstable Q point.

Example 2.6   In Example 2.5 if h_{FE} varies in the range $50 - 200$, calculate minimum and maximum values of I_C and V_{CE}.

Solution

(i) $h_{FE} = 50$

$$I_B = \frac{V_{CC} - 0.7}{R_B} = \frac{20V - 0.7V}{965 \ K\Omega} = 20 \ \mu A.$$

$$I_C = 50 \times 20 = 1000 \ \mu A = 1 \ mA.$$

$$V_{CE} = V_{CC} - I_C R_C = 20 - 1 \times 10^{-3} \times 2.2 \times 10^3$$

$$= 17.8 \ V$$

(ii) $h_{FE} = 200$

I_B will be same.

$$I_C = 200 \times 20 = 4000 \ \mu A = 4 \ mA$$

$$V_{CE} = 20 - 4 \times 10^{-3} \times 2.2 \times 10^3$$

$$= 11.2 \ V$$

Note that as h_{FE} increases, V_{CE} decreases and I_C increases, for same value of I_B. The range of I_C variation is $1 \ mA - 4 \ mA$. The range of V_{CE} is $11.2 \ V - 17.8 \ V$.

Base bias for pnp transistor

The base bias for *pnp* transistor is shown in Fig. 2.25(a). It is redrawn as shown in Fig. 2.25(b) to simply show $+ V_{CC}$ as supply source, instead of $- V_{CC}$.
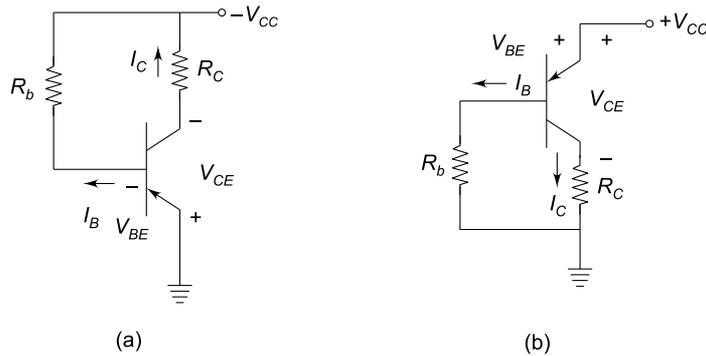
Fig. 2.25 *Base bias for pnp transistor*

The same equations can be used.

Example 2.7 A base bias circuit has $V_{CC} = 24$ V; $R_B = 390$ KΩ; $R_C = 3.3$ KΩ and $V_{CE} = 10$ V. Calculate transistor h_{FE} and determine new value of V_{CE} if a transistor with $h_{FF} = 100$ is used.

Solution

$$V_{CE} = V_{CC} - I_C R_C$$

$$10 = 24 - I_C \times 3.3 \times 10^3$$

$$I_C = \frac{24 - 10}{3.3 \times 10^3} = 4.24 \text{ mA.}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{24 - 0.7}{390 \times 10^3} = 59.74 \text{ μA}$$

$$h_{FE} = \frac{I_C}{I_B} = \frac{4.24 \times 10^{-3}}{59.74 \times 10^{-6}} = 70.97 \cong 71.$$

If it is replaced with a transistor of $h_{FE} = 100$, than I_B remains same.

$$I_C = h_{FE} I_B$$

$$= 100 \times 59.74 \text{ μA}$$

$$= 5.974 \text{ mA}$$

$$V_{CE} = 24 - 5.974 \times 10^{-3} \times 3.3 \times 10^3$$

$$= 4.2858 \text{ V.}$$

Example 2.8   A collector-to-base bias circuit has the following values: $R_B = 270$ kΩ; $R_C = 2.2$ kΩ; $V_{CC} = 18$ V and transistor $h_{FE} = 100$.

Solution

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + R_C (1 + h_{FE})}$$

$$= \frac{18 - 0.7}{[270 + 2.2 (1 + 100)] \times 10^3}$$

$$= 35.1 \ \mu A$$

$$I_C = h_{FE} I_B = 100 \times 35.1$$

$$= 3.51 \ mA$$

$$I_C + I_B = 3.51 \ mA + 35.1 \ \mu A = 3.5451 \ mA$$

$$V_{CE} = V_{CC} - R_C (I_C + I_B)$$

$$= 18 - 2.2 \times 10^3 (3.5451 \times 10^{-3})$$

$$= 10.2 \ V.$$

2.10.4   Voltage Divider Bias

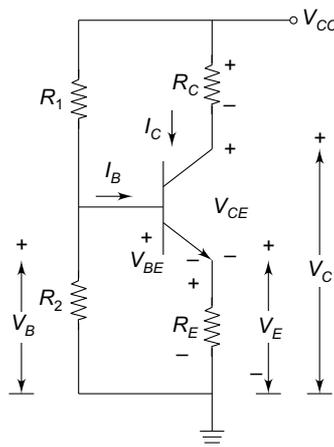The voltage divider bias circuit along with various voltages is shown Fig. 2.27.

Fig. 2.27   *Voltage divider bias*
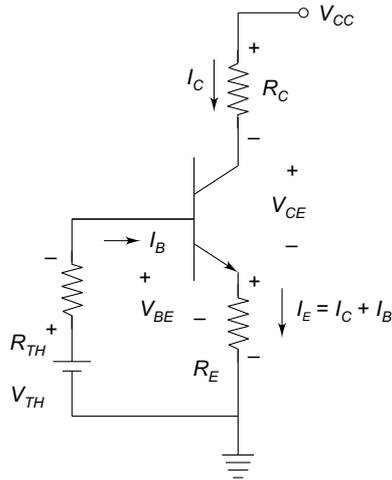
Fig. 2.28 *Exact circuit analysis of voltage divider bias*

From Fig. (2.28),

$$V_{TH} = I_B R_{TH} + V_{BE} + I_E R_E$$

$$= I_B R_{TH} + V_{BE} + (I_C + I_B) R_E \qquad (2.30)$$

Using $I_C = h_{FE} I_E$, we get

$$V_{TH} = I_B R_{TH} + V_{BE} + R_E I_B (1 + h_{FE})$$

From which

$$I_B = \frac{V_{TH} - V_{BE}}{R_{TH} + R_E (1 + h_{FE})} \qquad (2.31)$$

Once I_B is determined, $I_C = h_{FE} I_B$ and we can calculate V_{CE} as follows:

$$I_E = I_C + I_B$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E \qquad (2.32)$$

Example 2.9 A voltage divider circuit has the following values: $V_{CC} = 24$ V; $R_1 = 180$ kΩ; $R_2 = 56$ kΩ; $R_E = 4.7$ kΩ; $R_C = 8.2$ kΩ. Calculate approximate values of I_C, V_E, V_C and V_{CE}.

Solution

$$V_B = \frac{V_{CC} R_2}{R_1 + R_2} = \frac{24 \text{ V} \times 56 \text{ k}\Omega}{180 \text{ k}\Omega + 56 \text{ k}\Omega}$$

$$= 5.695 \text{ V}$$

$$V_E = V_B - V_{BE} = 5.695 - 0.7$$

$$= 4.995 \text{ V.}$$

(ii) Consider $h_{FE,\,max} = 250$

V_{TH} and R_{TH} remain the same.

$$I_B = \frac{5.695 - 0.7}{[42.71 + 4.7(1 + 250)] \times 10^3} = 4.08 \ \mu A$$

$$I_C = 250 \times 4.08 \ \mu A = 1.02 \ mA$$

$$I_E = I_C + I_B = 1.02 \ mA + 4.08 \ \mu A$$

$$= 1.024 \ mA$$

$$V_{CE} = 24 - 1.02 \ mA \times 8.2K - 1.024 \ mA \times 4.7K$$

$$= 10.82 \ V.$$

Hence

$$V_{CE,\,min} = 10.82 \ V$$

$$V_{CE,\,max} = 11.85 \ V.$$

We can see that the variation in V_{CE} is not much.

Example 2.11 In a voltage divider bias circuit $V_{CC} = 22$ V, $R_C = 10$ KΩ, $R_E = 1.5$ KΩ, $R_1 = 3a$ KΩ and $R_2 = 3.9$ KΩ. Determine the dc bias voltage and current using (i) approximate analysis and (ii) using exact analysis if β = 140.

Solution

(i) *Approximate analysis*

$$\beta R_E = 140 \times 1.5 \ K\Omega = 210 \ K\Omega$$

$$10 \ R_2 = 39 \ K\Omega.$$

Since $\beta R_E > 10 \ R_2$, we can use approximate analysis

$$V_B = \frac{V_{CC} R_2}{R_1 + R_2} = \frac{22 \times 3.9 \ k\Omega}{3.9 \ k\Omega + 39 \ k\Omega}$$

$$= 2 \ V.$$

$$V_E = V_B - V_{BE} = 2 - 0.7 = 1.3 \ V$$

$$I_E = \frac{V_E}{R_E} = \frac{1.3 \ V}{1.5 \ k\Omega} = 0.867 \ mA$$

$$I_C = I_E = 0.867 \ mA$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

$$= 22 - 0.867 \times 10^{-3}(10 + 1.5) \times 10^3$$

$$= 12.03 \ V.$$

(ii) *Exact Analysis*

$$V_{TH} = \frac{V_{CC}\,R_2}{R_1 + R_2} = 2\ \text{V}$$

$$R_{TH} = R_1\|R_2 = \frac{(39\ \text{K}\Omega \times 3.9\ \text{K}\Omega)}{39\ \text{K}\Omega + 3.9\ \text{K}\Omega}$$

$$= 3.55\ \text{K}\Omega$$

$$I_B = \frac{V_{TH} - V_{BE}}{R_{TH} + (\beta + 1)\,R_E}$$

$$= \frac{2 - 0.7}{3.55\ \text{k}\Omega + (140 + 1) \times 1.5\ \text{k}\Omega}$$

$$= 6.045\ \mu\text{A}$$

$$I_C = \beta I_B = 0.846\ \text{mA}$$

$$I_E = I_C + I_B$$

$$V_{CE} = V_{CC} - I_C\,R_C - I_E\,R_E$$

$$= 22 - 0.846 \times 10^{-3} \times 10 \times 10^3 - (0.846 + 0.0604) \times 1.5 \times 10^3$$

$$= 12.18\ \text{V}.$$

We can see that there is not too much of a difference between approximate analysis and exact analysis as tabulated below:

	I_C	V_{CE}
Exact	0.846 mA	12.18 V
Approximate	0.867 mA	12.03 V

Example 2.12 Given the device characteristics, Q point and load line, of a fixed bias circuit as shown in Fig. 2.30, determine V_{CC}, R_B R_C and h_{FE} of the transistor.
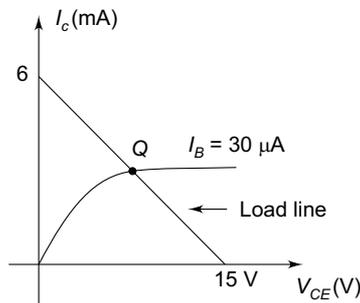

Fig. 2.29 *Example 2.13.*

Solution

The end points of the load line are $(V_{CC}, 0)$ and $\left(0, \dfrac{V_{CC}}{R_C}\right)$. Hence,

$$V_{CC} = 15 \text{ V}$$

$$I_C = \frac{V_{CC}}{R_C} = 6 \text{ mA}$$

$$R_C = \frac{15 \text{ V}}{6 \text{ mA}} = 2.5 \text{ K}\Omega$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$R_B = \frac{V_{CC} - V_{BE}}{I_B}$$

$$= \frac{15 \text{ V} - 0.7\text{V}}{30 \text{ μA}} = 476.67 \text{ K}\Omega$$

Standard resistor values close to 476.67 KΩ and 2.5 KΩ are 470 KΩ and 2.4 KΩ. So

$$R_C = 2.4 \text{ K}\Omega$$

$$R_B = 470 \text{ K}\Omega$$

$$I_B = \frac{15 \text{ V} - 0.7 \text{ V}}{470 \text{ k}\Omega} = 30.42 \text{ μA}$$

which is an error of 1.5%. Hence, it is acceptable.

Example 2.13   In a collector-to-base bias circuit $V_{CC} = 24$ V, $R_C = 3.3$ kΩ, $R_B = 180$ kΩ and $V_{CE} = 10$ V. Determine h_{FE}. Also determine V_{CE} when transistor is replaced by another one whose $h_{FE} = 120$. *(VTU July 2011)*

Solution

From eq. (2.18)

$$V_{CE} = V_{BE} + I_B R_B$$

$$I_B = \frac{V_{CE} - V_{BE}}{R_B}$$

$$= \frac{10 \text{ V} - 0.7 \text{ V}}{180 \text{ k}\Omega} = 51.67 \text{ μA}$$

In collector loop,

$$V_{CC} = (I_C + I_B) R_C + V_{CE}$$

$$= (1 + h_{FE}) I_B R_C + V_{CE}$$

$$24 = (1 + h_{FE}) 51.67 \times 10^{-6} \times 3.3 \times 10^3 + 10$$

$$= 0.1705 (1 + h_{FE}) + 10$$

$$h_{FE} = 81.1.$$

If it is replaced with another transistor with $h_{FE} = 120$, assuming same base current,

$$V_{CE} = V_{CC} - (1 + h_{FE}) I_B R_C$$

$$= 24 - (1 + 120) 51.67 \times 10^{-6} \times 3.3 \times 10^3$$

$$= 3.368 \text{ V}$$

Example 2.14   Determine the operating point of a silicon transistor with base bias having parameters: $\beta = 100$; $R_B = 500$ kΩ; $R_C = 2.5$ KΩ and $V_{CC} = 20$ V. Show the load line and the operating point on the load line.   *(VTU July 2011)*

Solution

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$= \frac{20 \text{ V} - 0.7 \text{ V}}{500 \text{ KΩ}}$$

$$= 38.6 \text{ μA}$$
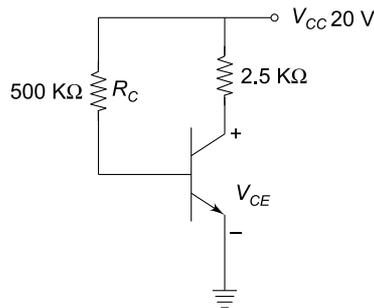
Fig. 2.30   *Example 2.15*

$$I_C = \beta I_B = 3.86 \text{ mA}$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$= 20 - 3.86 \times 10^{-3} \times 2.5 \times 10^3$$

$$= 10.35 \text{ V}$$

The coordinates of the load line are $\left(0, \dfrac{V_{CC}}{R_C}\right)$ and $(V_{CC}, 0)$ which are (0, 8 mA) and (20 V, 0)

The load line and the operating point are shown in Fig. 2.29.

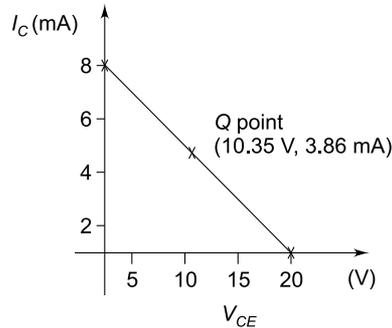**Fig. 2.31** *Solution of Example 2.15*

Example 2.15   The voltage divider bias circuit has V_{CC} = 15 V, R_1 = 6.8 KΩ, R_2 = 3.3 KΩ, R_E = 900 Ω R_C = 900 Ω and h_{FE} = 50. Find the levels of V_E, I_B, I_C, V_{CE} and V_C. Draw the dc load line and mark the *Q*-point on that.   *(VTU July 2013)*

Solution

$$V_B = \frac{V_{CC}\, R_2}{R_1 + R_2} = \frac{15 \times 3.3 \text{ KΩ}}{6.8 \text{ KΩ} + 3.3 \text{ KΩ}}$$

$$= 4.9 \text{ V}.$$

From eq. (2.23) $V_E = V_B - V_{BE}$

$$= 4.9 \text{ V} - 0.7 \text{ V}$$

$$= 4.2 \text{ V}$$

$$I_E = \frac{V_E}{R_E} = \frac{4.2 \text{ V}}{900 \text{ Ω}} = 4.66 \text{ mA}$$

$$I_C = I_E = 4.66 \text{ mA}$$

From eq. (2.27) $V_{CE} = V_{CC} - I_C (R_C + R_E)$

$$= 15 - 4.66 \times 10^{-3} (900 + 900)$$

$$= 6.61 \text{ V}$$

Since I_{CBO} approximately doubles every 10°C, if

$$n = \frac{\Delta T}{10}$$

then $$I_{CBO2} = I_{CBO1} \times 2^n \tag{2.38}$$

where I_{CBO1} is initial leakage current and I_{CBO2} is current after an increase in temperature of ΔT°C.

Example 2.17 Consider the following values: $R_1 = 33$ KΩ; $R_2 = 10$ KΩ; $R_C = 1$ KΩ; $R_B = 540$ KΩ $R_E = 1$ Ω; $h_{FE} = 75$. Calculate the stability factor for base-bias, collector-to-base bias and voltage divider bias, if these resistors are used in the circuits.

Solution

(i) Base bias

$$S = 1 + h_{FE} = 1 + 75 = 76$$

(ii) Collector-to-base bias

$$S = \frac{1 + h_{FE}}{1 + h_{FE}R_C/(R_C + R_B)}$$

$$= \frac{1 + 75}{1 + \left[\dfrac{75 \times 1 \text{ KΩ}}{1 \text{ KΩ} + 540 \text{ KΩ}}\right]}$$

$$= 66.7$$

(iii) Voltage divider bias

$$S = \frac{1 + h_{FE}}{1 + h_{FE}R_E/(R_E + R_1 \| R_2)}$$

$$= \frac{1 + 75}{1 + \dfrac{75 \times 1 \text{ KΩ}}{1 \text{ KΩ} + 33 \text{ KΩ} \| 10 \text{ KΩ}}}$$

$$= \frac{1 + 75}{1 + \dfrac{75 \times 1 \text{ KΩ}}{1 \text{ KΩ} + 7.67}} = \frac{76}{9.65}$$

$$S = 7.88.$$

We can observe that the voltage divider bias gives lowest value of S.

2.12 TRANSISTOR AS AN AMPLIFIER

The transistor amplifier circuit is shown in Fig. 2.34. Voltage divider bias circuit is used. If the input signal shifts the bias point from Q_0 to Q_1 and Q_2, the output current I_C and output voltage V_{CE} also vary as shown in Fig. 2.35.
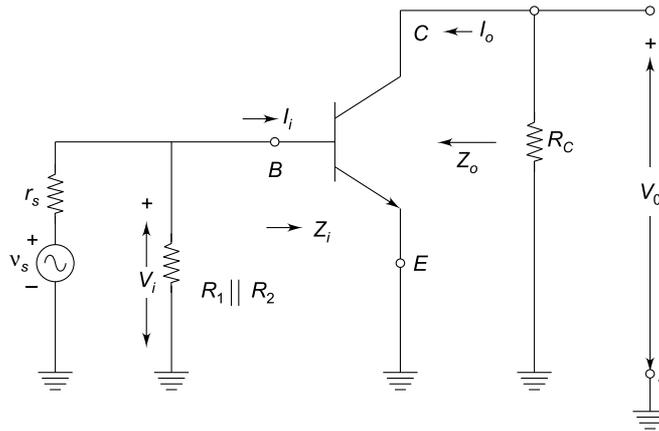
Fig. 2.37 *ac equivalent redrawn*

In Fig. 2.37 the voltage gain, A_v, is given by $\dfrac{V_0}{V_i}$ and current gain A_i, is given by $\dfrac{I_0}{I_i}$. The input current I_i is the base current, I_b (lower case b is used to denote ac quantity).
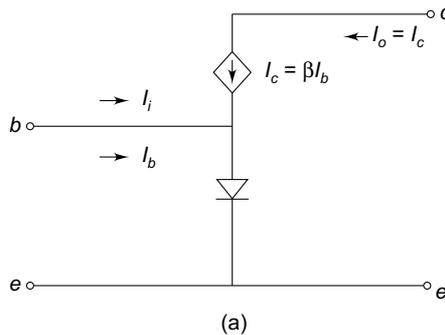
The transistor can be redrawn as shown in Fig. 2.38(a), with the base-emitter replaced by a diode, and the collector current I_C (which is also I_0) replaced by a current source βI_b. In Fig. 2.36(b), the diode is replaced by its forward dynamic resistance

$$r_e = \frac{26 \text{ mV}}{I_E} \tag{2.39}$$

$$I_e = I_C + I_b = (\beta + 1)\, I_b \text{ (for } (h_{fe} + 1)\, I_b)$$

Since β is >> 1, we can approximately say
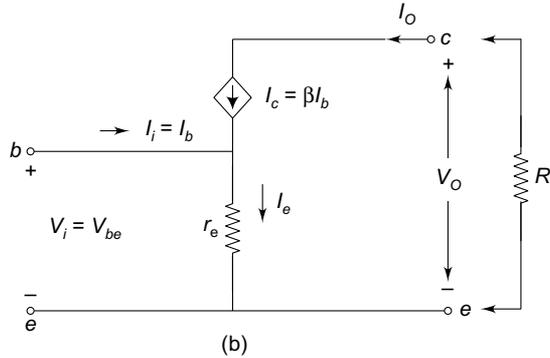
$$I_e \cong \beta I_b \tag{2.40}$$

(a)

Fig. 2.38   *Approximate model*

The input voltage $V_i = V_{be}$, from Fig. 2.38(b).

$$Z_i = \frac{V_i}{I_i}$$

Again from Fig. 2.36 (b),

$$V_{be} = I_e r_e = (I_C + I_b)\, r_e$$

$$= (\beta + 1)\, I_b\, r_e$$

$$I_i = I_b$$

$\therefore$
$$Z_i = \frac{(\beta + 1)\, I_b\, r_e}{I_b} = (\beta + 1)\, r_e \cong \beta r_e \tag{2.41}$$

The value of Z_i lies in the range of a few hundred ohms to around 6-7 KΩ. The output impedance Z_0 is obtained from common-emitter configuration output characteristics as,

$$\text{Slope} = \frac{1}{r_0}$$

The slope is not a constant and increases with increase in collector current. An increase in slope results in a decrease of the output impedance.

$$Z_0 = r_0$$

Z_0 lies in the range of 40 KΩ to 50 KΩ. If effect of r_o is neglected $Z_0 = \infty$. In Fig. 2.37 (b),

$$V_0 = -I_0\, R_L = -I_C R_L = -\beta I_b R_L$$

$$V_i = \beta I_b r_e$$

$$A_r = \frac{V_0}{V_i} = \frac{-\beta I_b R_L}{\beta I_b\, r_e} = \frac{-R_L}{r_e} \tag{2.42}$$

The negative sign indicates that output is out of phase with input signal.

$$A_i = \frac{I_0}{I_i} = \frac{I_c}{I_b} = \beta \tag{2.43}$$

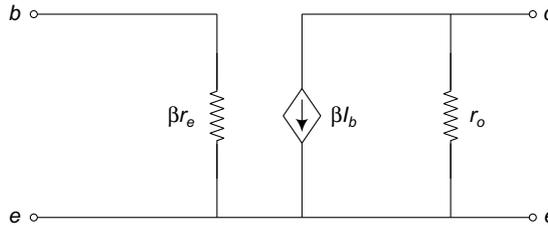The equivalent r_e model is shown in Fig. 2.37.

Fig. 2.39 *r_e model*

2.12.2 Decibel

The bel (B) is defined as

$$G = \log_{10} \frac{P_2}{P_1} \text{ bel} \tag{2.44}$$

This unit was found to be too large and a unit decibel (dB) was defined such that 10 decibels = 1 bel.

$$G_{\text{dB}} = 10 \log_{10} \frac{P_2}{P_1} \tag{2.45}$$

The rating of electronic communication equipment is often in decibels. The decibel defined above is the measure of difference in magnitude between two power levels. The power output P_2 is measured with respect to a reference power P_1. This is normally accepted to be 1 mW.

Decibel is also used for voltage gain as is given by

$$G_{\text{dB}} = 20 \log_{10} \frac{V_2}{V_1} \tag{2.46}$$

If we have a number of amplifiers in cascade the net gain is given by

$$G_{\text{dB}} = G_{\text{dB1}} + G_{\text{dB2}} + ... + G_{\text{dB}n} \cdot \text{dB}.$$

Example 2.18 If $\beta = 100$, and $I_E = 3$ mA for common emitter configuration with $Z_0 = \infty$ Ω, determine (i) z_i; (ii) A_v and A_i for a load of 1 kΩ

Solution:

(i) $r_e = \dfrac{26 \text{ mV}}{I_E} = \dfrac{26 \text{ mV}}{3 \text{ mA}} = 8.67 \ \Omega$; $z_i = \beta r_e = 100 \times 8.67 = 867 \ \Omega$

(ii) $A_v = \dfrac{-R_L}{r_e} = \dfrac{-1\text{K}\Omega}{8.67 \ \Omega} = -115.34$

$$A_i = \beta = 100.$$